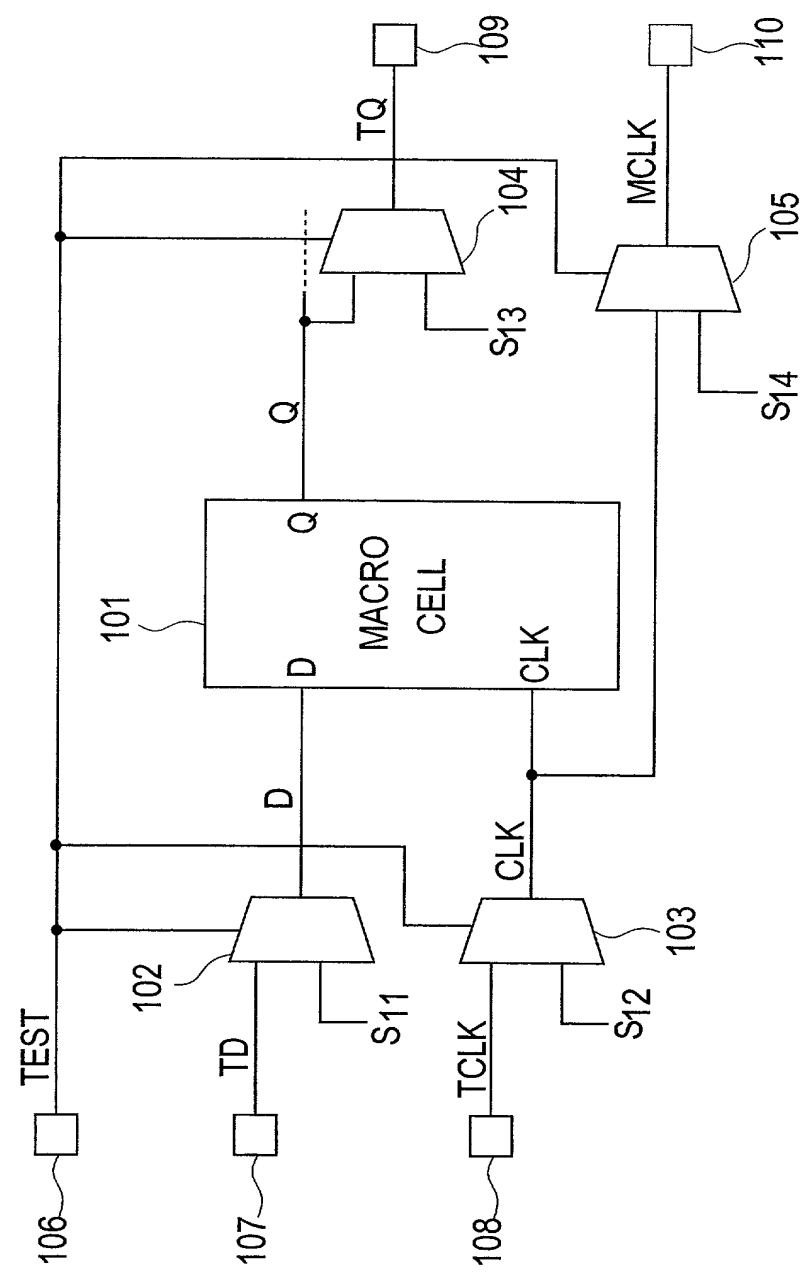


FIG. 1 is a block diagram of a macro cell in a system-on-chip (SOC) device. The macro cell 101 includes a data input/output (D) port, a clock (CLK) port, and a test data output (TQ) port. The D port is connected to a data bus 102 via a multiplexer 103. The CLK port is connected to a clock bus 104 via a multiplexer 105. The TQ port is connected to a test data output bus 106 via a multiplexer 107. The macro cell 101 is also connected to a test data input (TD) 108 and a test data output (TQ) 109. The test data input 108 is connected to the D port via a multiplexer 103. The test data output 109 is connected to the TQ port via a multiplexer 107. The macro cell 101 is also connected to a test data output (TQ) 109 via a multiplexer 107. The test data output 109 is connected to the TQ port via a multiplexer 107. The macro cell 101 is also connected to a test data output (TQ) 109 via a multiplexer 107. The test data output 109 is connected to the TQ port via a multiplexer 107.

FIG. 1



*FIG.2*

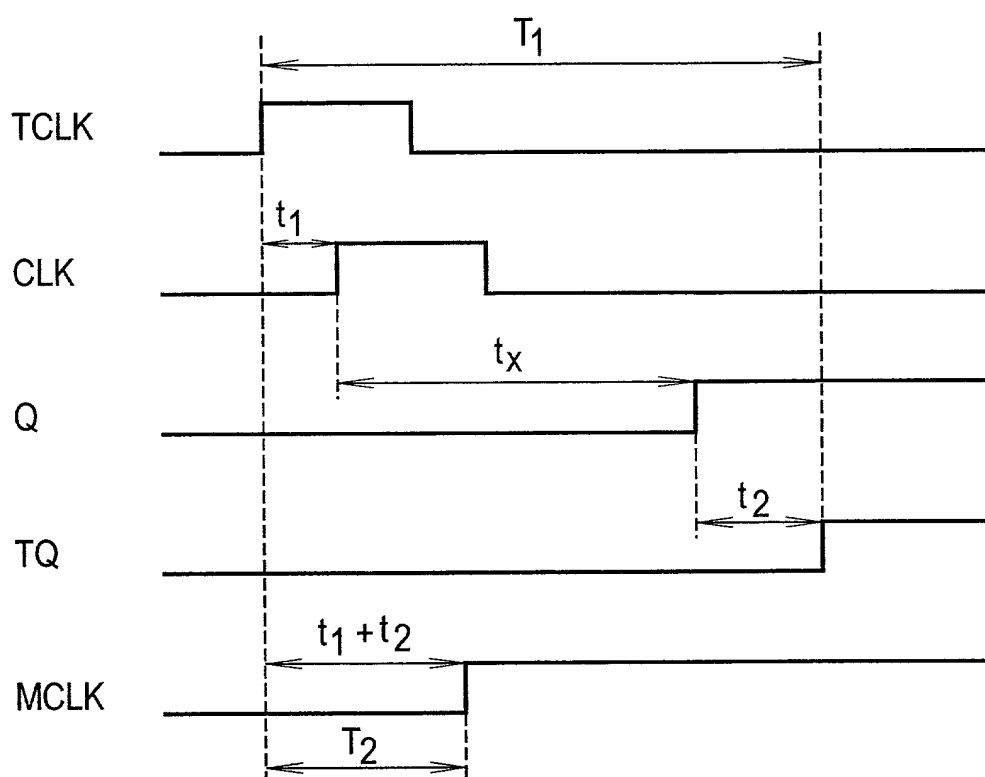


FIG. 3

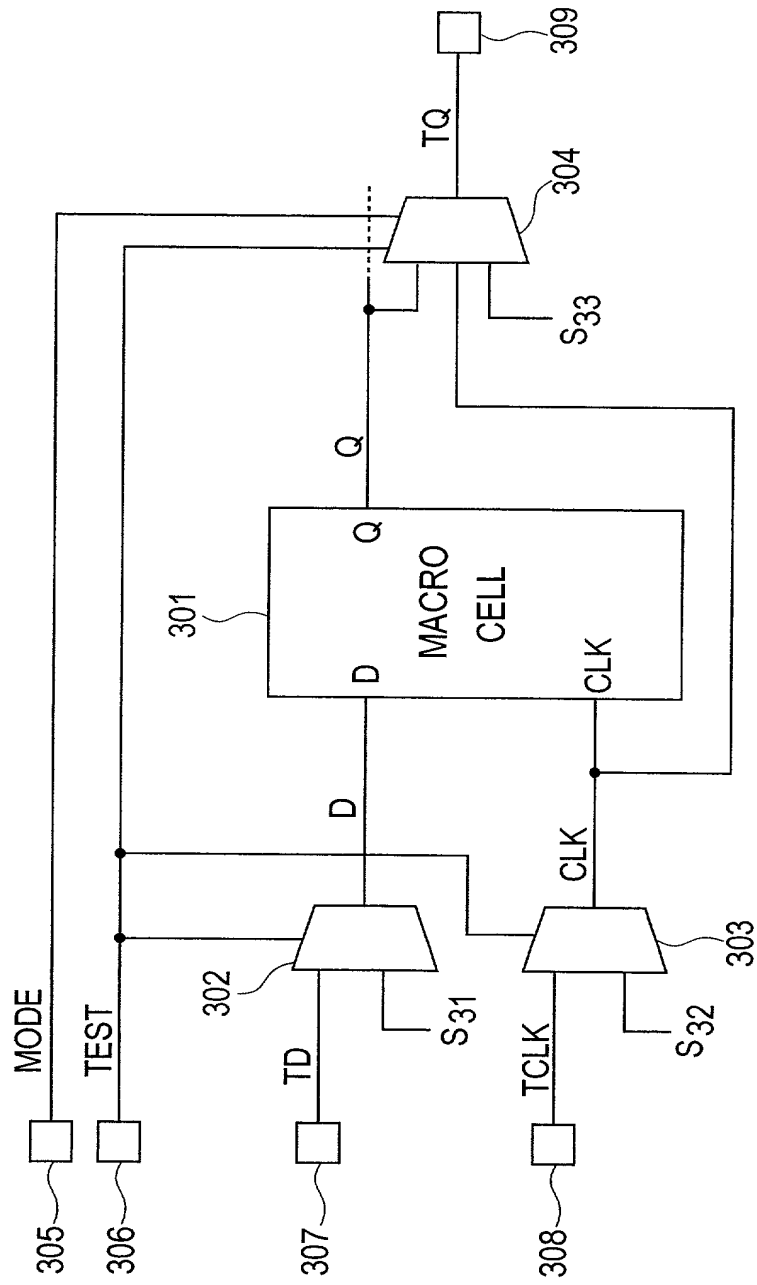


FIG. 4

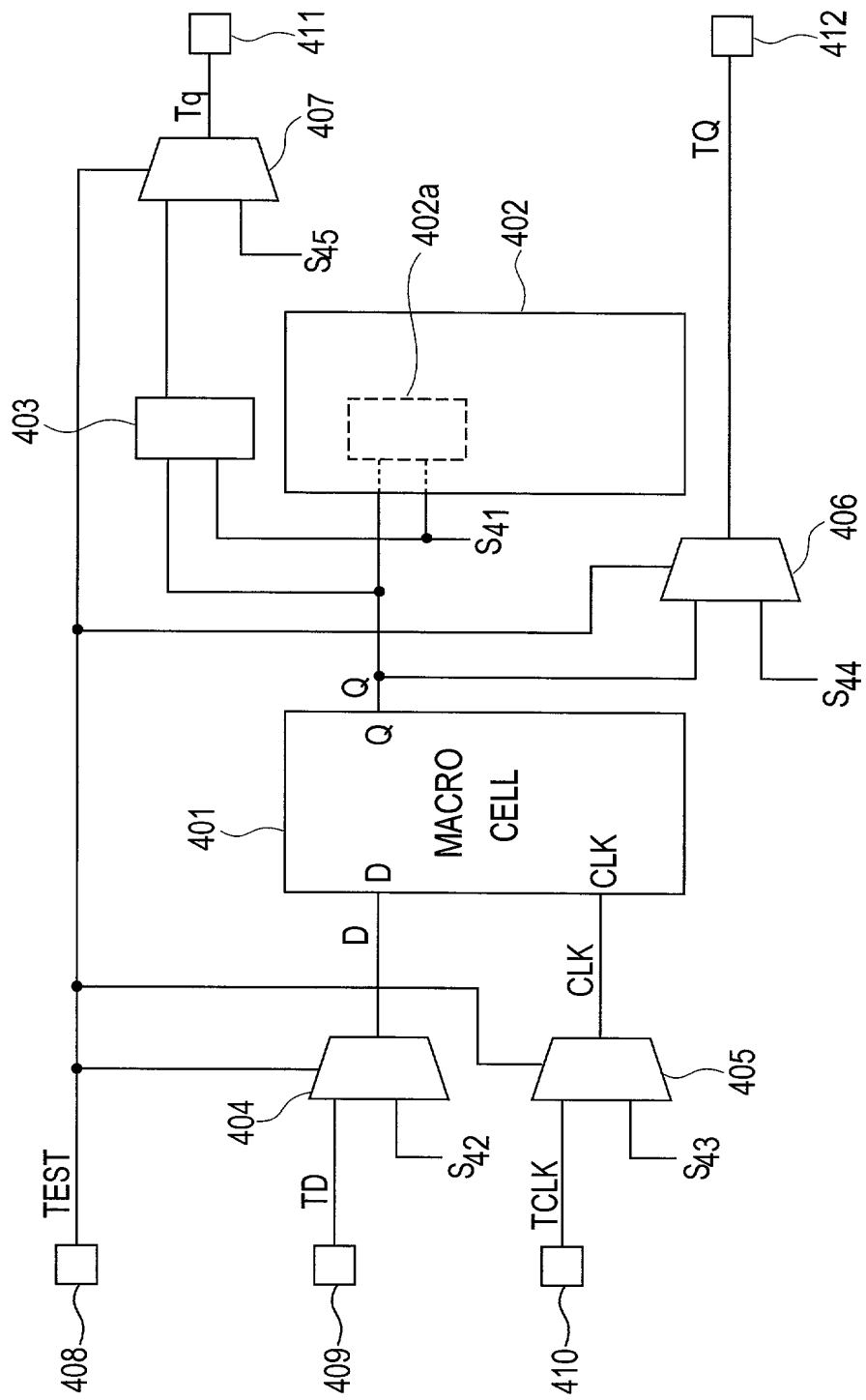


FIG. 5

